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10/673,211	09/30/2003	Xavier Montagne	003921.00136	9597

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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,211	MONTAGNE ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *9,11 and 21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 10, 12-20, 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. Applicants' Request for Continued Examination (RCE) and an amendment to the claims filed on 11/16/2007 have been entered.

2. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 2, 3, 4, 5, 6, 10, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farooq (US 6,760,277 B1) in view of Herron et al. (US 6,996,758 B1).

As per claim 1, Farooq teaches a method for testing configurable logic blocks in an emulation system, the method comprising steps of: operating a first set to test a second set of configurable logic blocks (fig. 2, col. 3, lines 8-42, Farooq).

However Farooq does not explicitly teach the specific use of configuring a first set of configurable logic blocks to be first testing circuitry; configuring each configurable logic block of the second set to respond with a deterministic output to an N-bit input, wherein the configuring the first set includes configuring a configurable logic block of the first set as a verifier to verify a responsive output of the second set organized into M groups of configurable logic blocks; wherein the verifier is configured to accept its own

output as one bit of the N-bit input, wherein, upon the output of the verifier being a failure indicator, the verifier is configured to maintain the failure indicator for the test.

Herron et al. in an analogous art teach that the test circuitry includes interconnect circuitry and test logic circuitry formed within the interfacing logic portion of the FPGA (fig. 9, col. 3, lines 41-44, Herron et al.). Herron also teaches that the test circuitry within the gasket...FPGA is operational (col. 3, line 57 to col. 4, line 3, Herron et al.). Herron teaches that according to one embodiment of a test operation...expected results (col. 4, lines 26-32, Herron et al.). Herron teaches that the output test vectors from the gasket logic are evaluated on the chip itself by logic within the FPGA fabric (col. 4, lines 38-40, Herron et al.). Herron teaches that in yet another embodiment, all output test vectors are evaluated on chip (col. 4, lines 42-43, Herron et al.). Herron et al. teach that the FPGA fabric is configured to analyze the test signal outputs received from the multiplexer to determine whether the fixed logic circuitry passed or failed the test (col. 10, lines 23-26, Herron et al.). Herron et al. teach that the FPGA fabric is configured to analyze the test signal outputs to determine whether the embedded core device passed or failed the test (col. 11, lines 18-20, Herron et al.). Herron et al. teach that the method includes receiving and evaluating the response from the device in the fixed interfacing logic to determine whether it has passed or failed (col. 22, lines 24-26, Herron et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Farooq's patent with the teachings of Herron et al. by including an additional step of configuring a first set of configurable logic blocks to be first testing circuitry; configuring each configurable logic block of the second set to respond with a deterministic output to an N-bit input, wherein the configuring the first set includes configuring a configurable logic block of the first set as a verifier to verify a responsive output of the second set organized into M groups of configurable logic blocks; wherein the verifier is configured to accept its own output as one bit of the N-bit input, wherein, upon the output of the verifier being a failure indicator, the verifier is configured to maintain the failure indicator for the test.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to configure the logic blocks to test other parts of the system.

- As per claim 2, Farooq and Herron et al. teach the additional limitations.

Herron et al. teach configuring the second set to be second testing circuitry (fig. 9, col. 3, lines 41-44, Herron et al.).

Farooq teaches operating the second set to test the first set (fig. 2, col. 3, lines 8-42, Farooq).

- As per claim 3, Farooq and Herron et al. teach the additional limitations.

Herron et al. teach configuring a third set of configurable logic blocks to be second testing circuitry (fig. 9, col. 3, lines 41-44, Herron et al.).

Farooq teaches operating the third set, concurrently with the first set, to test a fourth set of configurable logic blocks (fig. 2, col. 3, lines 8-42, Farooq).

- As per claim 4, Farooq and Herron et al. teach the additional limitations.

Herron et al. teach configuring the second set and the fourth set to be third testing circuitry and fourth testing circuitry, respectively (fig. 9, col. 3, lines 41-44, Herron et al.).

Farooq teaches operating the second set and the fourth set to test the first set and the third set, respectively (fig. 2, col. 3, lines 8-42, Farooq).

- As per claim 5, Farooq and Herron et al. teach the additional limitations.

Herron et al. teach the method, wherein the step of configuring the first set includes: configuring N.gtoreq.1 configurable logic blocks of the first set to operate as an N-bit input generator; and coupling an output of the N-bit input generator to the configurable logic blocks of the second set (col. 2, line 58-col. 3, line 3, col. 11, lines 51-56, Herron et al.).

- As per claim 6, Farooq and Herron et al. teach the additional limitations.

Herron et al. teach the method, further comprising a step of configuring a configurable logic block of the first set to determine whether the N-bit input generator outputs a predetermined value (col. 13, lines 44-54, Herron et al.).

- As per claim 10, Farooq and Herron et al. teach the additional limitations.

Herron et al. teach the method, wherein the verifier is configured to accept the N-bit input, and wherein each of the M groups includes N-1 configurable logic blocks configured to supply N-1 bits to the verifier (col. 4, lines 26-32, Herron et al.).

- As per claim 12, Farooq and Herron et al. teach the additional limitations.

Herron et al. teach the method; wherein the step of configuring the verifier includes configuring the verifier to deterministically output a failure indicator (col. 10, lines 23-26, col. 11, lines 18-20, col. 22, lines 24-26, Herron et al.).

6. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farooq (US 6,760,277 B1) and Herron et al. (US 6,996,758 B1) as applied to claim 6 above, and further in view of Kattan (US 6,621,767 B1).

As per claim 7, Farooq and Herron et al. substantially teach the claimed invention described in claim 6 (as rejected above).

However Farooq and Herron et al. do not explicitly teach the specific use of the method wherein the step of configuring the N >= 1 configurable logic blocks includes configuring the N >= 1 configurable logic blocks to operate as an N-bit counter.

Kattan in an analogous art teaches a 37-bit counter 212 in the FPGA (col. 12, line 16, Kattan).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Farooq's patent with the teachings of Kattan by including an additional step of using the method wherein the step of configuring the N >= 1 configurable logic blocks includes configuring the N >= 1 configurable logic blocks to operate as an N-bit counter.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to provide N-bit input to the second set of configurable logic blocks.

- As per claim 8, Farooq, Herron et al. and Kattan teach the additional limitations.

Kattan teaches the method, wherein the predetermined value is a maximum value of the N-bit counter (col. 12, line 16, Kattan).

7. Claims 13, 14, 15, 16, 17, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Butts et al. (US 5,036,473) in view of Cote et al. (US 6,470,485 B1) and Flanagan et al. (US 6,141,334).

As per claim 13, Butts et al. teach configuring a first routing portion to map N inputs of the first routing portion to N outputs of the first routing portion in a first configuration; the N inputs of the second routing

portion configured to be coupled to the N outputs of the first routing portion; applying input data to the inputs of the first routing portion; and receiving output data from the output of the second routing portion, the output data being responsive to the input data (fig. 3, col. 2, lines 15-19, col. 11, lines 46-50, col. 12, lines 30-37, col. 13, lines 5-35, Butts et al.).

However Butts et al. do not explicitly teach the specific use of a method of testing routing portions in an emulation system.

Cote et al. in an analogous art teach that the ability of all parts of the interconnect within the IC...proper operation of the integrated circuit (col. 1, lines 59-64, Cote et al.). Cote et al. also teach that testing of interconnect resources...fully operational (col. 2, lines 16-27, Cote et al.). Cote et al. teach that a simulation model of the FPGA under-test is constructed with its logic blocks configured to implement sequencers such as shown in FIG. 2A (col. 13, lines 18-20, Cote et al.). Cote et al. teach to efficiently test all of the diversified interconnect resources of the FPGA embodiment 300 (fig. 3A, col. 18, lines 58-60, Cote et al.). Cote et al. teach test-enabling reconfigurations of the FPGA 300...interconnect is free of defects (col. 19, lines 28-60, Cote et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Butts et al.'s patent with the teachings of Cote et al. by including an additional step of using the method of testing routing portions in an emulation system.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the method of testing routing portions in an emulation system would provide the opportunity to verify that all parts of the interconnect within the IC correctly and consistently route all signals in timely and accurate fashion between configurable logic blocks.

Butts et al. also do not explicitly teach the specific use of configuring a second routing portion to map N inputs of the second routing portion to N outputs of the second routing portion in a second configuration inverse to the first configuration.

Flanagan et al. in an analogous art teach that a second NxN switch (not shown) is interposed between the multipliers and the respective combiners to ensure that the appropriate multiplier products are routed

to the proper combiners. The second NxN switch advantageously performs the inverse routing of NxN switch 500 and can be also controlled by switch controller 501, in well-known fashion (fig. 5, col. 8, lines 3-9, Flanagan et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Butts et al.'s patent with the teachings of Flanagan et al. by including an additional step of configuring a second routing portion to map N inputs of the second routing portion to N outputs of the second routing portion in a second configuration inverse to the first configuration.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to provide required routing of signals to the system elements.

- As per claim 14, Butts et al., Cote et al. and Flanagan et al. teach the additional limitations.

Cote et al. teach the method, further comprising a step of determining whether a difference exists between the input data and the output data (fig. 3A, col. 19, lines 57-60, Cote et al.).

- As per claim 15, Butts et al., Cote et al. and Flanagan et al. teach the additional limitations.

Cote et al. teach the method, further comprising a step of configuring a first group of configurable logic blocks to perform the step of applying, wherein the configurable logic blocks include logic circuitry for implementing reprogrammable logic (fig. 1B, col. 5, lines 47-48, Cote et al.).

- As per claim 16, Butts et al., Cote et al. and Flanagan et al. teach the additional limitations.

Cote et al. teach the method, further comprising a step of configuring a second group of configurable logic blocks to perform the step of determining (col. 9, lines 44-46, Cote et al.).

- As per claim 17, Butts et al., Cote et al. and Flanagan et al. teach the additional limitations.

Cote et al. teach the method, wherein the N inputs of the second routing portion are configured to be coupled to the N outputs of the first routing portion through at least one reconfigurable interconnect (fig. 1B, col. 7, lines 2-8, Cote al.).

- As per claim 23, Butts et al., Cote et al. and Flanagan et al. teach the additional limitations.

Butts et al. teach an integrated circuit, comprising: a first routing portion configured to map N inputs of the first routing portion to N outputs of the first routing portion in a first configuration, and configured to

receive input data; wherein the N inputs of the second routing portion are coupled to the N outputs of the first routing portion (fig. 3, col. 2, lines 15-19, col. 11, lines 46-50, col. 12, lines 30-37, col. 13, lines 5-35, Butts et al.).

Flanagan et al. teach a second routing portion configured to map N inputs of the second routing portion to N outputs of the second routing portion in a second configuration inverse to the first configuration, and configured to output data (fig. 5, col. 8, lines 3-9, Flanagan et al.).

Cote et al. teach monitoring logic configured to determining whether a difference exists between the input data and the output data (fig. 3A, col. 19, lines 57-60, Cote et al.).

8. Claims 18-20, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cote et al. (US 6,470,485 B1) in view of Lesea (US 6,874,107 B2).

As per claim 18, Cote et al. teach an integrated circuit, comprising: a first set of configurable logic blocks; a second set of configurable logic blocks, coupled to the first set; and a data processing portion coupled to the first set, the data processing portion configured to provide a first test pattern to the first set, wherein the first set is configured to provide a second test pattern to test the second set, and the second set is configured to output data in response to the second test pattern received from the first set, wherein the first set is further configured to provide an N-bit input generator to the second set (fig. 3B, 3C, 4A, 4B, col. 1, lines 10-13, col. 17, line 66 to col. 18, line 3, col. 23, lines 48-50, col. 24, lines 1-17, col. 25, lines 6-26, col. 25, lines 33-47, col. 26, lines 35-42, col. 27, lines 9-13, lines 18-40, Cote et al.).

However Cote et al. do not explicitly teach specifically to provide a configurable logic block, separate from the N-bit input generator, as a verifier to verify the output data of the second set.

Lesea in an analogous art teaches that a field programmable gate array (FPGA) comprises input and output data communication connections, a serializer/deserializer circuit coupled to the input and output data communication connections, and a logic array programmed to generate a test data pattern coupled to the output data connection. The logic array is further programmed to check a data pattern received on the input connection while performing a built in self test operation (fig. 2, col. 2, lines 34-42, Lesea).

Lesea teaches that a method of testing...memory circuit of the FPGA (col. 6, lines 54-67, Lesea).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Cote et al.'s patent with the teachings of Lesea by including an additional step of providing a configurable logic block, separate from the N-bit input generator, as a verifier to verify the output data of the second set.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to verify interconnect boards including integrated circuits so that the signals can be routed correctly.

- As per claim 19, Cote et al. and Lesea teach the additional limitations.

Cote et al. teach the integrated circuit, wherein the first set is further configured to compare the output data to predetermined output data (fig. 3C, col. 25, lines 6-26, Cote et al.).

- As per claim 20, Cote et al. and Lesea teach the additional limitations.

Cote et al. teach the integrated circuit, wherein the data processing portion is further configured to provide a third test pattern to the second set, the second set is further configured to provide a fourth test pattern to test the first set, and the first set is further configured to output second data in response to fourth test pattern received from the second set (fig. 3B, 3C, 4A, 4B, col. 23, lines 48-50, col. 24, lines 1-17, col. 25, lines 33-47, col. 26, lines 35-42, col. 27, lines 18-30, Cote et al.).

- As per claim 22, Cote et al. and Lesea teach the additional limitations.

Cote et al. teach the integrated circuit, wherein an output of the verifier is an input to the verifier, and wherein the output of the verifier is a failure indicator (fig. 3C, col. 25, lines 6-26, Cote et al.).

9. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng et al. (US 5,903,744) in view of Cote et al. (US 6,470,485 B1).

As per claim 24, Tseng et al. teach an emulation system, comprising: a plurality of emulation boards; and a plurality of interconnect boards interconnecting the plurality of emulation boards (fig. 1, col. 1, line 51-col. 2, line 16, Tseng et al.).

However Tseng et al. do not explicitly teach the specifically that each of the plurality of interconnect boards has an integrated circuit having first and second sets of configurable logic blocks and a data processing portion coupled to the first and second sets, wherein the data processing portion is configured

to provide a first test pattern to the first set to test the second set and a second test pattern to the second set to test the first set.

Cote et al. in an analogous art teach that FIG. 3C shows another implementation in accordance with the invention. The feedback loop of an FPGA-implemented sequencer need not comprise just one VGB and its adjacent interconnect resources. A loop can be composed of plural VGB's (fig. 3C, col. 25, lines 6-10, Cote et al.). Cote et al. teach that FIG. 3C shows just VGB-A and VGB-M positioned within a feedback loop (col. 25, lines 12-13, Cote et al.). Cote et al. teach creating different excitational patterns in various segments of each of the testing loops (col. 25, lines 19-21, Cote et al.). Cote et al. also teach computerized testing system 400...packaged IC device (fig. 4A, col. 25, lines 34-47, Cote et al.). Cote et al. teach a method for interconnecting components...processors (fig. 4B, col. 26, lines 36-43, Cote et al.). Cote et al. teach FPGA configuring...test-result reports (col. 27, lines 19-40, Cote et al.). Cote et al. also teach to provide computer-understandable instructions to computers for causing the computers to perform automated stepping of FPGA's under-test through a battery of reconfigurations and test loops and readouts (col. 27, lines 57-60, Cote et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tseng's patent with the teachings of Cote et al. by including additionally that each of the plurality of interconnect boards has an integrated circuit having first and second sets of configurable logic blocks and a data processing portion coupled to the first and second sets, wherein the data processing portion is configured to provide a first test pattern to the first set to test the second set and a second test pattern to the second set to test the first set.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to verify interconnect boards including integrated circuits so that the signals can be routed correctly.

10. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng et al. (US 5,903,744) in view of Butts et al. (US 5,036,473), Cote et al. (US 6,470,485 B1) and Flanagan et al. (US 6,141,334).

As per claim 25, Tseng et al. teach an emulation system, comprising: a plurality of emulation boards; and a plurality of interconnect boards interconnecting the plurality of emulation boards (fig. 1, col. 1, line 51-col. 2, line 16, Tseng et al.).

However Tseng et al. do not explicitly teach specifically that each of the plurality of interconnect boards has an integrated circuit having first and second routing portions, wherein the first routing portion is configured receive input data and to map N inputs of the first routing portion to N outputs of the first routing portion in a first manner, wherein the second routing portion is configured to output data.

Butts et al. in an analogous art teach that logic chips...realized logic (col. 11, lines 46-50, Butts et al.). Butts et al. also teach that route the interconnections...accomplish the interconnect (col. 12, lines 30-37, Butts et al.). Butts et al. teach that the channel-routing interconnect...alternating logic and routing chips (col. 13, lines 6-27, Butts et al.). Butts et al. also teach that an "interconnect chip" is an electronically reconfigurable device which can implement arbitrary interconnections among its I/O pins. A "routing chip" is an interconnect chip used in a direct or channel-routing interconnect (col. 2, lines 15-19, Butts et al.).06

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tseng's patent with the teachings of Butts et al. by including additionally that each of the plurality of interconnect boards has an integrated circuit having first and second routing portions, wherein the first routing portion is configured receive input data and to map N inputs of the first routing portion to N outputs of the first routing portion in a first manner, wherein the second routing portion is configured to output data.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to route signals in the interconnect boards so that the emulation boards can be interconnected.

Tseng et al. also do not explicitly teach specifically that the monitoring logic is configured to determining whether a difference exists between the input data and the output data.

However Cote et al. in an analogous art teaches that eight independent feedback paths...free of defects (fig. 3A, col. 19, lines 57-60, Cote et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tseng's patent with the teachings of Cote et al. by including additionally that the monitoring logic is configured to determining whether a difference exists between the input data and the output data. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to find defects in the interconnect so that the signals can be routed correctly using a fault-free interconnect.

Tseng et al. also do not explicitly teach specifically that the second routing portion is configured to map N inputs of the second routing portion to N outputs of the second routing portion in a second manner inverse to the first manner.

Flanagan et al. in an analogous art teach that a second NxN switch (not shown) is interposed between the multipliers and the respective combiners to ensure that the appropriate multiplier products are routed to the proper combiners. The second NxN switch advantageously performs the inverse routing of NxN switch 500 and can be also controlled by switch controller 501, in well-known fashion (fig. 5, col. 8, lines 3-9, Flanagan et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tseng et al.'s patent with the teachings of Flanagan et al. by including an additional step of the second routing portion configured to map N inputs of the second routing portion to N outputs of the second routing portion in a second manner inverse to the first manner.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to provide required routing of signals to the system elements.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dipakkumar Gandhi
Patent Examiner

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